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REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Amendments to the claims

The preamble of claims 1 – 6 have been amended to precisely describe the feature of the instant application as "the post-etch wet cleaning process." This amendment is fully supported by Para [0021] of the instant application, which recites the following: "Each of the semiconductor wafers 10 has a main surface comprising at least one exposed copper metal feature 22 or 24 as set forth in Fig.1" and further supported by Fig. 1, which shows a post-etch dual damascene structure. Therefore, the key feature of the instant application includes **a post-etch wet cleaning process.** Accordingly, the amended preamble of claims 1 – 6 is fully supported by the specification.

Claim Rejections – 35 U.S.C. 112 and 35 U.S.C. 102(b)

Claims 7 – 11 were rejected under 35 U.S.C. 112, first paragraph, and claims 7, 9 and 11 were rejected under 35 U.S.C. 102(b) as being anticipated by Bryan C. Chung.

Response

Claims 7 – 11 have been cancelled.

Claim rejections – 35 U.S.C. 103(a)

Claims 1 – 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bryan C. Chung (hereafter Chung) in view of A. Beverina et al. (hereafter Beverina).

Response

Claim 1

Claim 1 has been amended to include the following patentable feature: "a wafer having a main surface comprising at least one copper metal feature, a dielectric film formed on the copper metal feature and at least one opening formed in the dielectric film, wherein at least a portion of the copper metal feature is exposed through the opening". The amended claim 1 emphasizes that the wafer undergoes the cleaning step **after the via/trench dry etch** and therefore **has a Cu metal feature exposed through the opening of the dielectric film**. In addition, the wafer with the structure (a Cu metal feature exposed through the dielectric film) is called a **post-etch dual damascene structure** (Para [19]). The above claim amendment is fully supported by Fig. 1, as well as Para [0019] of the instant application. Para [0019] recites: "a recess 13 formed due to the Cu loss is observed at a **top surface** of a first level metal", which inherently teaches that there is an opening so a top surface can be observed. Therefore, the amended claim 1 is fully supported by the specification.

The examiner alleged that Chung does not teach that water comprises an exposed copper feature and a dielectric film. (See office action dated Dec. 4, 2007, page 5).

Beverina merely teaches a **damascene structure**, and a **post-CMP cleaning** process to clean the copper **after a CMP process**. However, the amended claim 1 features that the wafer includes a **damascene structure** which is covered by a dielectric film, and at least one opening is formed in the dielectric film, wherein at least a portion of the copper metal feature is exposed through the opening." In other words, the wafer includes a **post-etch dual damascene structure**. Moreover, the cleaning process taught in the instant application is **a post-etch cleaning**. That is, **the cleaning process is carried out after the via/trench is formed by a dry etch.** Therefore, the cited references either alone or in combination fail to teach the timing at which the **post-etch cleaning** is performed, and also fail to teach the **post-etch dual damascene structure.**

The examiner alleged that Chung teaches "cleaning said main surface of said wafer by contacting a cleaning solution in said light inhibited manner" (See office action dated Dec. 4, 2007, page 4).

Chung teaches a dark spin rinse to eliminate the galvanic corrosion. The galvanic corrosion is produced during the rinsing/drying process. As those skilled in the art should know, the rinsing process is a step usually performed after the wet etch or the wet cleaning process (Col. 1, lines 25-30). After the rinsing process is performed, the inert gas is used to dry up the wafer (Col. 2, lines 1-7). The **water used in the rinsing process is de-ionized water** (Chung, Col. 1, lines 64-65).

However, the mechanism of galvanic corrosion taught by Chung is totally different from the mechanism of photovoltaic corrosion taught in the instant application. Moreover, the amended claim 1 of the instant application limits that the wafer is cleaning by contacting **a cleaning solution** in the light inhibited manner. The cleaning solution includes **HF**, **H_2O_2**, **NH_4OH** etc. (Para [6]). Therefore, the solution used in the rinsing of Chung is totally different from the cleaning solution taught in the instant application. As a result, Chung fails to teach "cleaning said main surface of said wafer by contacting **a cleaning solution** in said light inhibited manner" as required in the amended claim 1. Accordingly, the cited references either alone or in combination fail to establish a prima facie case of the instant application.

With all these arguments considered, the amended claim 1 should by patentable over the prior arts. Reconsideration of the amended claim 1 is politely requested.

Response

Claims 2 – 6

As claims 2 – 6 are dependent upon claim 1, they should be allowable if claim 1 is allowed.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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/ Winston Hsu / Date: 01.29.2008

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